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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,104	08/17/2001	Eiji Yoshida	212881US2	3616

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OBLON SPIVAK MCCLELLAND MAIER & NEUSTADT PC
FOURTH FLOOR
1755 JEFFERSON DAVIS HIGHWAY
ARLINGTON, VA 22202

EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 07/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/931,104	YOSHIDA, EIJI	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *4,8-10 and 12-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 1-3, 5-7 and 11 (Group I, Embodiment I) in Paper No. 5 is acknowledged. The traversal is on the ground(s) that searches of device and method claims overlap, and hence no serious burden to the examiner is involved in searching both method and device claims. This is not found persuasive because the purpose, i.e., finding prior art based on device casu quo method criteria for identifying prior art, of the search as well as the domain of the search (class and subclass within which the search has to be carried out), are different. Applicant has not directed his traverse to the specific grounds put forward by the examiner on which the restriction/election requirement was based.

The requirement is still deemed proper and is therefore made FINAL.

Drawings

2. Figure 11 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. ***Claims 1, 2*** are rejected under 35 U.S.C. 102(b) as being anticipated by Prior Art as Admitted by Applicant in the disclosure of his invention.

With regard to claim 1: with reference to Prior Art Figure 11, Applicant discloses on pages 2-5 of his disclosure a semiconductor device (see also title), comprising: a portion (indicated as "peripheral circuit" in Figure 11) to be measured by fluctuation in potential; a wire 12 having one (lower) end and the other end connected with said portion to be measured; and an observation part (regions 3 and 5 and their pn junction) connected with said one end of said wire, wherein said observation part includes a pn junction (pn junction between regions 3 and 5) irradiated with a laser beam (one of the two near-infrared laser beams 20 indicated in Figure 11) to detect said fluctuation in potential, and said pn junction includes a first impurity region 3 of a first conductivity type (n-type) connected with said one end of said wire and a second impurity region 5 of a second conductivity type (p-type). In conclusion, Prior Art as admitted by Applicant anticipates claim 1.

With regard to claim 2: said first impurity region 3 is formed within said second impurity region 5 (cf. Figure 11).

With regard to claim 3: said observation part includes a first MOS transistor (n channel MOS transistor 110) having said first impurity region as a source/drain region (drain region 3).

With regard to claim 5: the semiconductor device further comprises a second MOS transistor 120 including said portion (said peripheral circuit) to be measured,

wherein said first MOS transistor and said second MOS transistor are arranged in a same gate array, namely: the gate array of the CMOS device.

With regard to claim 7: said portion to be measured comprise a source/drain region of said second MOS transistor 120, namely drain region 4.

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. ***Claim 1*** is rejected under 35 U.S.C. 102(a) as being anticipated by Tsang et al (Proc. IEEE, Volume 88, No.9, September 2000; especially Section IX, page 1455).

With regard to claim 1: Referring to Section IX of their Paper, page 1455, and Figure 18, Tsang et al teach a semiconductor device (cf. title and abstract of Invited Paper), comprising: a portion (indicated by white arrow, which is the output wire of the CMOS device; see legend of Figure 18) to be measured by fluctuation in potential; a wire (the bottom of which is connected to the impurity region illuminated by the laser beam) having one end, and the other end connected with said portion to be measured; and an observation part (the region illuminated by the laser beam) connected with said one end of said wire, wherein said observation part includes a pn junction irradiated with a laser beam to detect said fluctuation in potential, and said pn junction includes a first impurity region of first conductivity type (n-type) connected with said one end of said wire and a second impurity region of a second conductivity type (p substrate). In conclusion, Tsang et al anticipate claim 1.

With regard to claim 2: said first impurity region (indicated n+) is formed within said second impurity region (p-substrate).

With regard to claim 3: said observation part includes a first MOS transistor having said first impurity region as a source/drain region, namely as drain region of the p-channel MOS within the CMOS device.

With regard to claim 5: the device by Tsang et al further comprises a second MOS transistor including said portion to be measured (said portion is common among the p-channel and n-channel MOS devices making up the CMOS transistor), wherein said first MOS transistor and said second MOS transistor are arranged in a same gate array, namely the gate array of the CMOS transistor.

With regard to claim 7: said portion to be measured comprises a source/drain region of said second MOS transistor, namely the drain region of the p-channel MOS device within the CMOS transistor.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. ***Claims 6 and 11*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant in his disclosure, and, in the alternative, over Tsang et al (Proceedings of the IEEE, Volume 88, No.9, September 2000, pages 1440-1459; especially page 1455 and Figure 18). As detailed above, claim 5, on which claim 6 depends, is anticipated by Prior Art Admitted by Applicant in the disclosure of his

invention on pages 2-5 and through Figure 11, and, in the alternative, anticipated by the journal article in the Proceedings of the IEEE by Tsang et al. Although the disclosure by Applicant and the publication by Tsang fail to specifically teach that said portion to be measured is a gate electrode of said second MOS transistor, the gate electrode of said second MOS transistor is actually tested in view of the following observations:

Said portion to be measured (peripheral circuit) comprises the gate electrode of said second MOS transistor: see for instance the wire 11 in Applicant's disclosure connecting said gate electrode 1 to the peripheral circuit, and without which there would be no point testing the said gate electrode, as it would simply be a floating gate or piece of conductive material, not hooked up to perform a function extraneously imposed upon it. To check functions one needs the function signal capability, which is enabled by the connection to said peripheral circuit through said wire 11. Should the gate function be disabled, then the laser probe of region 3 would confirm the n-channel of MOS transistor 110 to be closed under all settings of the gates. Therefore, said portion to be tested also comprises a gate electrode of said second MOS transistor.

With regard to claim 11: As detailed above, claim 1 (on which claim 11 depends) is anticipated by Prior Art as Admitted by Applicant in the disclosure of his invention (pages 2-5 and Figure 11). Furthermore, the semiconductor device of claim 1 as taught by the Prior Art Admitted by Applicant in the disclosure of his invention indeed discloses said first conductivity type to be n-type and said second impurity region to be p-type; said observation part further includes a second pn junction having a p-type third impurity region 4 connected with said wire 12 and an n-type fourth impurity region 7; and a first

fixed potential is applied to said second impurity region, namely ground (i.e., zero) 8 as applied through wire 13, and a second fixed potential different from said first fixed potential is applied to said fourth impurity region, namely the power source supply potential 9.

Although said disclosure does not necessarily teach the second fixed potential to be higher than the aforementioned first fixed potential, said second fixed potential certainly is higher in magnitude than ground, as ground is zero by definition. Furthermore, it is understood by those of ordinary skills in the art that CMOS devices such as described as Prior Art in the disclosure of Applicant's invention on pages 2-5 and through Figure 11 are best known for their application as inverters. A typical input voltage to the gates when lower than the n-channel threshold voltage and sufficiently negative with respect to the bulk of the p-channel MOSFET 120 will turn said p-channel MOSFET on, whereby a conducting p-channel path is created to the power source supply while the n-channel MOSFET 110 is turned off, which yields a positive output voltage, being the common drain voltage. Hence, in this operational mode the aforementioned second fixed potential is higher than ground, i.e., higher than said first fixed potential.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Kash et al (5,940,545); Wai Mun Yee et al (Proceedings of the 1999 7th International Symposium on the Physical and Failure Analysis of Integrated Circuits, 5-9 July 1999; pages 15-19, Singapore; ISBN: 0-7803-5187-8).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
June 29, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800